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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/937,194	09/21/2001	Seiji Ohno	NSG-201US	6387

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EXAMINER
MONDT, JOHANNES P

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 04/23/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/937,194	OHNO ET AL.	
	Examiner	Art Unit	
	Johannes P Mondt	2826	

-- *The MAILING DATE f this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2003 and 21 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,6,7 and 10-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,6,7 and 10-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continu d Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/17/2003 has been entered as Paper No. 12.

Response to Amendment

Amendment B filed 01/21/2003 has been entered as Paper No. 9 in light of the Request for Continued Examination (Paper No. 12). Applicant canceled claims 4, 5 and 9. In view of the previous cancellation of claims 2, 3 and 8 the following claims are in the application: claims 1, 6, 7, 10 and 12-14. Applicant substantially amended claims 1, 6, 7, 11 and 12, and thereby all outstanding claims either directly or indirectly through their dependence on independent claims 1, 6, 7 or 11. Comments on Remarks by Applicant in said Amendment B are included below under "Response to Arguments".

Response to Arguments

Remarks by Applicant have been fully considered but are not persuasive. In particular, Applicant states on page 10 of said Amendment B that it is Applicant's contention that the light-emitting thyristor array of [the new] claim 1 is patentably distinguished from the references of record at least on the basis on (of?) the feature that "when a prime factor for N is 2 only, the number of gate-selecting lines is positive and is

the smallest integer, the next smaller integer, or third smaller integer that satisfies the expression L / {N/M + M} > p." Here, p is the pitch of the bonding pads, M is the number of gate-selecting lines, and N is the number of thyristors, while L is the length of the long side of the chip, along which long side the thyristors form an array. The said feature, the "Prime Factor Feature" in Applicant's nomenclature, is, however, automatically satisfied for small $N=2^q$, q integer, $q \leq 3$, as is evident from first principles and finds embodiment in, for instance, Kusuda (JP403194978A), Figure 1, for which Figure n (the said N) is a variable for which 4 is allowed as it is any even natural number. It is clear that for N=4 M=2 minimizes the expression N/M+M and hence would be either the smallest or next smaller number as defined in the claim. Therefore, although no specific embodiments have been found for 8 or more thyristors, for which the range implied by the Prime Factor Feature is necessarily overlapped by the prior art, and although no obviousness argument has been found based on other prior art for said Prime Factor Feature, the patentability of it has to be constrained to values for N that are at least 8 (i.e., exceed 4 and must have 2 only as prime factor).

Analogously, turning now to claims 6 and 11, for the case when both 2 and 3 are prime factors of N and M is selected to be equal to 2, as disclosed by Kusuda for instance (Figure 1, n can be any even number), it is clear that the selection n=6 as comprised by Kusuda corresponds to a minimizing value of $6^{1/2}$ for m in the real domain. It so happens that N/M + M has the same value for M=2 and M=3 in the case when N=6, and hence M=2 must be the smallest plurality for which the minimum value of

N/M+M is achieved. Therefore, the value N=6 must be excluded from the claim language of claims 6 and 11.

The following art rejections are based on the above critical considerations.

Drawings

2. Figure 15 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. ***Claims 1, 6 and 12*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Prior Art as Admitted by Applicant (henceforth called "APA") in view of Kamei (JP359117280A), Sonobe et al (US 2002/0153532 A1), and Kusuda (JP403194978A) (listed in IDS of Paper No. 4).

As shown in the disclosure on pages 2 and 3, and as illustrated in Figure 1, APA teaches a light-emitting thyristor matrix array formed on a chip (page 2, lines 7-8 and page 3, line 9) comprising:

N (N being an integer > 1) three-terminal (anode, cathode, gate) light-emitting thyristors (page 2, lines 9, 12, 14, and 16) in one line (page 2, line 10) in parallel with the long side of the chip (all thyristors are positioned on said chip while they are aligned with (along) the long side of the chip);

a common terminal to which cathodes are of the N light-emitting thyristors are connected (indicated "K" on Figure 1 and page 2, lines 15-16);

M (M=4>1) gate-selecting lines (cf. Figure 1 and page 2, lines 17-20);

a plurality of bonding pads also formed on the chip (cf. page 3, line 8-10);

wherein the gate of the k-th light-emitting thyristor is connected the i-th (modulus M=4) gate-selecting line G_i, the anode being connected to the j-th anode terminal A_j, where j= (k-i)/M +1;

APA does not necessarily teach the plurality of bonding pads to be arrayed in one line in parallel with the long side of the chip. However, Kamei teaches a plurality of bonding pads arrayed in one line in parallel with the long side of the chip, namely bonding pads 9a (Figures 1 and 2). The purpose of Kamei, namely to facilitate adjusting the trimming (adjusting the light amount) through a separate bonding pad 9a for each light-emitting element 5, enabling the option of separate re-connecting of any light-emitting element to an alternative bonding pad (bonding pads 9b, 9c, etc.), is a valid *motivation* also for the invention disclosed as Prior Art admitted by Applicant because the intensities of different printing lines should ideally be the same. Furthermore, the distance between each light-element 5 and its bonding pad 9a, casu quo alternative

bonding pads 9b, 9c,.., is kept minimal by means of the alignment of bonding pads 9a in parallel with the light-element array.

Kamei does not necessarily teach the plurality of bonding pads to be a plurality of {M/N+M} bonding pads. However, APA teaches {N/M + M} control terminals (namely M control terminals for the M gate selecting lines and one control terminal for each of the N/M sub-groups of thyristors) in the conventional art as disclosed on page 2 of the disclosure (lines 25-30), while Sonobe et al teach that, with as *motivation* by the cost and space saving advantage of reducing positional deviations in the area of the control circuit substrate (cf. sections [0020] and [0062]), each control terminal 3c is folded in an L-shape to correspond or form a bonding pad 4c (cf. section [0076]). Said *motivation* is sufficiently generic to also constitute motivation to combine the teaching in this regard by Sonobe et al into the invention of the APA. Sonobe et al thereby make it *obvious* that the number of bonding pads can be made advantageously to equal the number of control terminals in the invention of Kamei in order to improve the capitalization of surface area while preserving the integrity of the connections.

Also, the light-emitting thyristor essentially taught by APA in view of Kamei satisfies the further limitation that L/p > M/N +M, because Kamei shows that there is ample room for (at least) one more bond pad to be placed on the chip, and thus the length L exceeds the product of the number of bond pads and the pitch of the bond pad array by more than one bond array pitch. It is understood in the art that to place the absolute maximum number of elements in an array as allowed by the length of the chip would place the outer elements arbitrarily close to outside influence.

The inventions can be straightforwardly *combined* in as far as the relevant aspects of the teachings by Kamei and Sonobe et al are concerned, because the linear array of light-emitting elements as taught by the APA is simply the first step in the manufacturing process for the end product. Reasonable expectation of success is ensured by the absence of any unknown elements in the manufacturing process and in the independence of the fabrication of the array of light-emitting elements and the array of bonding pads.

Finally, although neither the APA, nor Sonobe et al, nor Kamei necessarily teach the final three lines of claim 1, it can be shown that for small enough N (=number of thyristors) M inescapably satisfies the further limitation of the final three lines (henceforth called "Prime Factor Feature", following the Applicant). The Prime Factor Feature is automatically satisfied for $N=2^q$, q integer, $q < 3$, as is evident from first principles and finds embodiment in, for instance, Kusuda (JP403194978A), Figure 1, for which Figure n (the said N) is a variable for which 4 is allowed as it is any even natural number. It is clear that for N=4 the selection in Kusuda for M, i.e., M=2, minimizes the expression N/M+M and hence would be the smallest number as defined in the claim while more than 4 gate-selecting lines would not even be necessary in any design in this case. It is clear, therefore, that the "Prima Factor feature" defines a range for M and N that partly overlaps with that found in the prior art. Applicant is reminded that a prima facie case of obviousness typically exists when the ranges of a claimed composition overlaps the ranges disclosed in the prior art or when the ranges of a claimed composition does not overlap but are close enough such that one skilled in the art

would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Motivation to incorporate the teaching by Kusuda in this regard is prompted by those applications in which 4 light-emitting thyristors suffice; only the selection of N is involved here, which clearly is a matter dictated by the luminous yield per thyristor and the total yield needed. *Combination* of the teaching in this regard by Kusuda with the invention only requires the selection of the number of thyristors and does not affect any other aspect of the invention. *Success* in implementing the combination can therefore be reasonably expected.

With regard to claim 6: the same teaching by Kusuda, Figure 1, includes the selection n(=N)=6, while the value of N/M + M for M=2 equals said value for M=3, namely 6/2 + 2 = 6/3 + 3 = 5, whilst the minimum over all real values for M of N/M + M resides at $M = N^{1/2}$, which equals 2.45; hence it is clear that, combined with the remainder of the limitations, the teaching by Kusuda of the selection of 6 thyristors and 2 gate-selecting lines provides either the smallest value for M, and hence the further limitation involved here defines a range that partly overlaps with the one found in the prior art. Applicant is reminded that a prima facie case of obviousness typically exists when the ranges of a claimed composition overlaps the ranges disclosed in the prior art or when the ranges of a claimed composition does not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. In re Peterson, 65 USPQ2d 1379 (CA FC 2003).

Motivation for said selections as taught by Kusuda stems from the application for which the thyristors are meant, i.e., the selection of the necessary luminous yield, while having more than the minimum number of gate-selecting lines would be an unnecessary cost burden. *Combination* of the teaching by Kusuda in this regard with the invention is straightforwardly achieved by mere selection of the number of thyristors and the number of gate-selecting lines with altering any other feature of the invention. *Success* in the implementation of said invention can therefore be reasonably expected.

With regard to claim 12: Any of the claims 2-6 are unpatentable over APA in view of Kamei and Sonobe et al, as explained above. Although a driver circuit has not necessarily been disclosed as APA nor by Kamei nor by Sonobe et al nor by Kusuda, a driver circuit for the aforementioned gate-selecting lines as well as a driver circuit for driving the aforementioned anode terminals are inherent for these gate-selecting lines and anode terminals in light of their function. It is equally obvious that the very process of selecting a gate to receive a signal implies for the relevant circuit to output a "selecting" signal to one of the gate-selecting signal output terminals and a "no-selecting" signal to the other gate-selecting signal output terminals, with the terminal to which the "selecting" signal is supplied being switched in turn. The very meaning of the word "selecting" suffices here.

3. ***Claims 13-14*** are rejected under 35 U.S.C. 103(a) as being unpatentable over APA, Kamei, Sonobe et al and Kusuda as applied to claim 12 above, and further in view of Mead et al (5,763,909). Although neither APA nor Kamei nor Sonobe nor Kusuda disclose the further limitation as defined in claim 13 it is understood that the selection of

parallel or serial input / output registers is a matter of design choice, as discussed by Mead et al in connection with a phototransistor imaging system, hence in the field of the invention (cf. title, abstract and column 10, lines 1-14), for which Mead specifically argues for a serial in the case of analog multiplexing, and specifically states the choice at hand generally to be a design choice (column 10, line 14). Motivation to include the teaching by Mead in the case of analog multiplexing is thus specifically taught by Mead; combinability only involves a serial electrical arrangement, at no consequence to the remainder of the invention. Success in implementing the teaching by Mead in this regard is thus reasonably expected.

With regard to claim 14: the number of the gate-selecting signal output signal terminals in the APA must be four since there are four gate-selecting lines. The further limitation as defined by claim 14 therefore does not distinguish over the prior art.

4. ***Claims 7 and 10*** are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art, in view of Kamei (JP359117280A), Sonobe et al (US 2002/0153532 A1), Kusuda (JP403194978A), and Breeze (5,394,653).

On those features that are common between claims 1 and 10, and claim 7 please be referred to the reasons for rejection of claim 1 as amply expanded above. Neither APA nor Kamei necessarily teach the specific limitation of claim 7 not included in claim 1. However, in the art of light-emitting element arrays for image display systems (cf. title and abstract), hence closely related to the art of the invention, Breeze teaches (cf. Fig. 3) LED arrays in which a there is a spatial period characterized by a fixed number of adjacent LEDs, each member of said fixed number of LEDs corresponding to

a different image (cf. column 2, line 38 – column 3, line 6); the total image is then a superposition of images produced by the members of said fixed number of LEDs, while image selection is carried out through the anode voltage selection (cf. Fig. 3; cf. column 4, line 66 – column 5, line 63). The anode connection is different for every different member of said fixed number of LEDs, i.e., within the spatial period, while the gates within the period are interconnected ohmically. For the usefulness of the invention as taught by APA in view of Kamei as defined in claim 1 for the purpose of image display it therefore would be obviously advantageous to have separate anodes but a common gate within the LED periodic unit responsible for the display of one character. Therefore, there is ample *motivation* to combine the inventions. Identically the same advantageous spatial arrangement of electrical connections with the aim of reducing connection requirements on spatial resources would be achieved when the commonality of the anode would be replaced by the commonality of the gate. The inventions can be *combined*: all that needs to be done is to *interchange* anode and gate connections without loss of said spatial resources. *Reasonable expectation of success is ensured* keeping in mind the relative simplicity involved in the interchange.

In conclusion, it would have been obvious to one of ordinary skills in the art to modify the invention of claim 1 (as essentially taught by APA and Kamei) so as to include the further limitation as defined by claim 7.

5. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art, in view of Kamei (JP359117280A), Sonobe et al (US 2002/0153532 A1), Kusuda (JP403194978A), and Breeze (5,394,653).

On those limitations that are common between claims 7 and 11 please be referred to the reasons for rejection of claim 1 as amply expanded above. These common limitations comprise all but the final three lines. As detailed above, claim 7 is unpatentable over APA in view of Kamei, Sonobe et al, Kusuda and Breeze.

With regard to the further limitation described in the final three lines of claim 11: The teaching by Kusuda, Figure 1, includes the selection n(=N)=6, while the value of N/M + M for M=2 equals said value for M=3, namely 6/2 + 2 = 6/3 + 3 = 5, whilst the minimum over all real values for M of N/M + M resides at $M = N^{1/2}$, which equals 2.45; hence it is clear that, combined with the remainder of the limitations, the teaching by Kusuda of the selection of 6 thyristors and 2 gate-selecting lines provides either the smallest value for M.

Motivation for said selections as taught by Kusuda stems from the application for which the thyristors are meant, i.e., the selection of the necessary luminous yield, while having more than the minimum number of gate-selecting lines would be an unnecessary cost burden. *Combination* of the teaching by Kusuda in this regard with the invention is straightforwardly achieved by mere selection of the number of thyristors and the number of gate-selecting lines with altering any other feature of the invention. *Success* in the implementation of said invention can therefore be reasonably expected.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P Mondt whose telephone number is 703-306-0531. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 703-308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JPM
April 20, 2003

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